

Abstract of the Disclosure

Increasing need to gain higher performance and lower power in semiconductor chips and field programmable gate arrays requires that optimization be done in a constructive manner with respect to physical layout. Increasing performance by parasitic budgeting which dictates what parasitics are acceptable to meet timing and power goals is presented. Providing these controls allows the physical implementation system to skew connection parasitics in a way that makes critical components and their connections significantly faster than those in the rest of the circuit. This represents a unique advantage of existing methods and provides a unique method to reach higher levels of performance and lower power than existing approaches.

15

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Ronald Craig Fish, President
Ronald Craig Fish a Law Corporation
Reg. No. 28,843